REMARKS

This paper is responsive to the Office Action dated December 31, 2004. All rejections and objections of the Examiner are respectfully traversed. Reconsideration and further examination is respectfully requested.

At paragraphs 1 and 2 of the Office Action, the Examiner objected to the Specification for having boldfaced section headings. Amendments to the Specification are believed to meet all requirements of the Examiner in this regard.

At paragraph 3 of the Office Action, the Examiner objected to claims 5-18 based on certain informalities. Amendments to the claims are believed to satisfy all requirements of the Examiner in this regard.

At paragraph 4 of the Office Action, the Examiner rejected claim 17 as being a "substantial duplicate" of claim 16. Claim 17 has been canceled.

At paragraphs 5 and 6 of the Office Action, the Examiner rejected claims 1-3, 5-6 and 9-18 under 35 U.S.C. 102(e), citing United States patent number 6,157,955 of Narad et al. ("Narad et al."). Applicants respectfully traverse this rejection.

Narad et al. disclose a general-purpose programmable packet-processing platform for accelerating network infrastructure applications, which have been structured so as to separate the stages of classification and action. As described in Narad et al., network packet classification, execution of actions upon those packets, management of buffer flow, encryption services, and management of Network Interface Controllers may be accelerated through the use of a multiplicity of specialized modules. See Abstract.

In the Narad et al. system, to support atomic enqueueing/dequeueing of buffer pointers and of DMA (Direct Memory Access) descriptors pointers, a memory-based producer/consumer ring structure is supported in hardware for passing pointers to data between producer and consumer processes. Narad et al. teach that a Media Access Control receive ring has an associated Produce Pointer for the process that allocates empty buffers, a MAC FILL Pointer for the Receive Media Access Control process that consumes empty buffers and also produces full buffers, a Classification Engine Consume Pointer for a process that consumes received buffers and produces classified buffers, and a Policy Processor Consume Pointer for a process that consumes classified packets. See Fig. 6 of Narad et al. Narad et al. further describe providing a leading producer process with an "enqueue" register for accessing the ring, and a "dequeue" register for an end consumer process to access the ring for synchronization purposes. See column 11, lines 12-25.

Narad et al. describe a "Crypto Command Queue" and "General Purpose Communication Rings" that are used to schedule buffers for processing by an encryption engine. This memory-based ring contains buffer pointers, and is supported by enqueue and dequeue operations, and a status bit indicating that there is at least one packet buffer pointer in the ring to process. See column 26, line 65 through column 27 line 7.

With regard to the DMA (Direct Memory Access) functionality, the Narad et al. system includes a "DMA Command Queue and Descriptors". The DMA engine of Narad et al. uses a ring unit with an Enqueue register for any agent to schedule DMA transfers, a Consume register for the DMA engine to get entries from the ring, and a Dequeue register for recovering retired descriptors from the ring. DMA operations are scheduled by creating a 16-byte descriptor in

memory and then enqueueing the address of that descriptor in the DMA engine's command ring. See column 28, lines 10 through 24.

Narad et al. describe per packet software data structures used to carry information about corresponding stored packets. This data structure includes a timestamp value representing a time that the stored packet was received, and a status word was written describing the received packet. The format of the status word in this data structure includes a number of bit flags at specific positions within the status word, as well as fields describing source, length and offset attributes of the stored packet. See column 22, lines 9-45 and Table 1.

As defined within the packet STATUS word used to describe a packet stored in memory of the Narad et al. system, an offset field describes where the start of a stored packet within a buffer, and enables an agent process to manipulate headers and relocate the start of the packet header as needed. Zero-filled two-byte pads may be inserted prior to the start of the packet header, or the system can transmit a packet starting at any arbitrary byte alignment in the transmit buffer of Narad et al. See column 24, lines 50 through 64.

In the Narad et al. programming model, the Narad et al. platform is to be considered a service, provided within a network, that may require direct knowledge or manipulation of network packets or frames. The Narad et al. programming model is described as providing "direct access" to low-level frame data, plus a set of library functions capable of reassembling low-level frame data into higher-layer messages or packets, and of performing protocol operations on network or transport-layer messages. See column 59, lines 39-50.

Nowhere in Narad et al. is there disclosed or suggested any system or method for direct access to bit fields in instruction operands, including:

providing ***indications of bit fields in source and target operands of a processor executable instruction***, each of the indicated bit fields consisting of a plurality of bits in a plurality of bit positions;

performing the processor executable instruction utilizing the bit fields in the source and target operands in response to the indications of the bit fields; and

providing, by the performing the processor executable instruction, and in response to the indications of the bit fields, direct manipulation of any bits in any bit field of the source and target operands. (emphasis added)

As in the present independent claim 1. Analogous features are also set forth in the present independent claim 5. In contrast, Narad et al. describe a system including rings of pointers for passing control of buffers indicated by the pointers, a status word including bit field definitions for indicating the status of a packet stored in memory buffers, a data structure that also may be used to store information about stored packets, and a programming model for providing access to stored packet data as a service. Sections of Narad et al. cited in the Office Action, and discussed above, describe definitions of bit fields *in a status word reflecting the status of a packet in memory buffers*. The use of bit definitions in a status word or control register is far different from the indications of bit fields in source and target operands of a processor executable instruction, as set forth in the present independent claims 1 and 5. Nothing in the programming model description in section V of Narad et al. teaches even the desirability of the presently claimed bit field indications for bit fields in source and target operands of a processor executable instruction of claims 1 and 5. Moreover, in the description of the Classification Engine (Section IV beginning at line 38 of Column 36), Narad et al. teach the use of dedicated functionality to perform masking and rotating of data prior to its use within operands. Beginning at line 26 of Column 37, Narad et al. state as follows:

. . . A mask-and-rotate unit allows arbitrary bit fields to be extracted from words of the packet ***which can then be used as operands in computation or as comparison values for bulk table comparisons***. (emphasis added)

Thus the system of Narad et al. uses a mask-and-rotate unit to pre-process data to be used in operands in computations. That approach of Narad et al. stands in clear contradistinction to the present independent claims 1 and 5, in which ***indications of bit fields within source and target operands of a processor executable instruction are used to define bit fields at any location within the source and target operands themselves.***

For the above reasons, Applicants respectfully urge that Narad et al. does not disclose or suggest all the features of the present independent claims 1 and 5. Accordingly, Applicants respectfully urge that Narad et al. does not support a *prima facie* case of obviousness under 35 U.S.C. 103 with regard to independent claims 1 and 5. With regard to claims 2-3, 6 and 9-18, they each depend from claims 1 and 5, and are respectfully believed to be patentable over Narad et al. for at least the same reasons.

In paragraphs 7-9 of the Office Action, the Examiner rejected claims 4 and 7-8 for obviousness under 35 U.S.C. 103, again citing Narad et al., in combinations with United States patent publication number 2003/0035430 A1 of Islam et al. ("Islam et al."), and United States patent publication number 2002/0174318 A1 of Stuttard et al. ("Stuttard et al."). As neither Islam et al. nor Stuttard et al. include any teaching regarding bit field processing, Applicants respectfully urge that the combinations Narad et al. with Islam et al. and Stuttard et al. also fail to disclose or suggest any system or method for direct access to bit fields in instruction operands, including:

providing ***indications of bit fields in source and target operands of a processor executable instruction,*** each of the indicated bit fields consisting of a plurality of bits in a plurality of bit positions;

performing the processor executable instruction utilizing the bit fields in the source and target operands in response to the indications of the bit fields; and

providing, by the performing the processor executable instruction, and in response to the indications of the bit fields, direct manipulation of any bits in any bit field of the source and target operands. (emphasis added)

As in the present independent claims 1 and 5, from which claims 4 and 7-8 depend. Accordingly, Applicants respectfully urge that the cited combinations of Narad et al. with Islam et al. and Stuttard et al. fail to provide a *prima facie* case of obviousness under 35 U.S.C. 103 with regard to independent claims 1 and 5, and that dependent claims 4 and 7-9 are patentable over the combined references for at least the same reasons.

Reconsideration of all pending claims is respectfully requested, and Applicants respectfully request that all rejections and objections be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone David A. Dagg, Applicants' Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

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